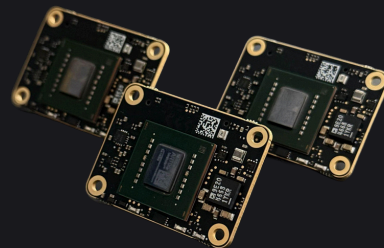


OEM TIMING MODULE

WHITE RABBIT
MEZZANINE

DATASHEET



INTRODUCTION

The White Rabbit Mezzanine Board is an OEM-focused timing module which exists alongside the Open Time Node, based on White Rabbit for deterministic, phase-aligned timing in distributed systems. The Mezzanine is intended for integrators requiring precise synchronisation across multiple endpoints, designed to extend and distribute ultra-precise synchronisation throughout complex environments. Equipped with four independent White Rabbit ports, it seamlessly integrates into networks to deliver sub-nanosecond accuracy.

KEY FEATURES

- White Rabbit compatible deterministic ethernet timing for multi-node synchronisation
- Sub-nanosecond class synchronisation capability
- Low jitter local timing outputs for precision measurements and control applications
- OEM-oriented hardware architecture with compact integration footprint
- Host accessible timing telemetry for lock status, monitoring and diagnostics
- 4 independent SFP cages for White Rabbit networking

CONNECTORS OVERVIEW

- 10M IN — 10 MHz input from grandmaster (COAX)
- CAL — Calibration input / Measurement port (COAX)
- PPS_IN — 1PPS reference input from grandmaster (COAX)
- PPS_OUT (A1-A4) — 1PPS outputs aligned to master when locked
- 10M_OUT (A1-A4) — 10 MHz output, phase locked via PLL
- P12V — 12V DC barrel jack • USB-C for management

White Rabbit

Sub-ns Sync

4x SFP

1PPS In/Out

10 MHz

OEM Module



MEASURED PERFORMANCE

JITTER ANALYSIS

TIMING PRECISION & STABILITY

JITTER PERFORMANCE

Sample Count	61,816 period samples
Mean Period	25.73 ns (38.87 MHz)
RMS Jitter (std dev)	24.67 ps
Peak-to-Peak Spread	200.2 ps
IQR	34.18 ps
Gaussian-fit Sigma	26.77 ps

TIMING OUTPUTS

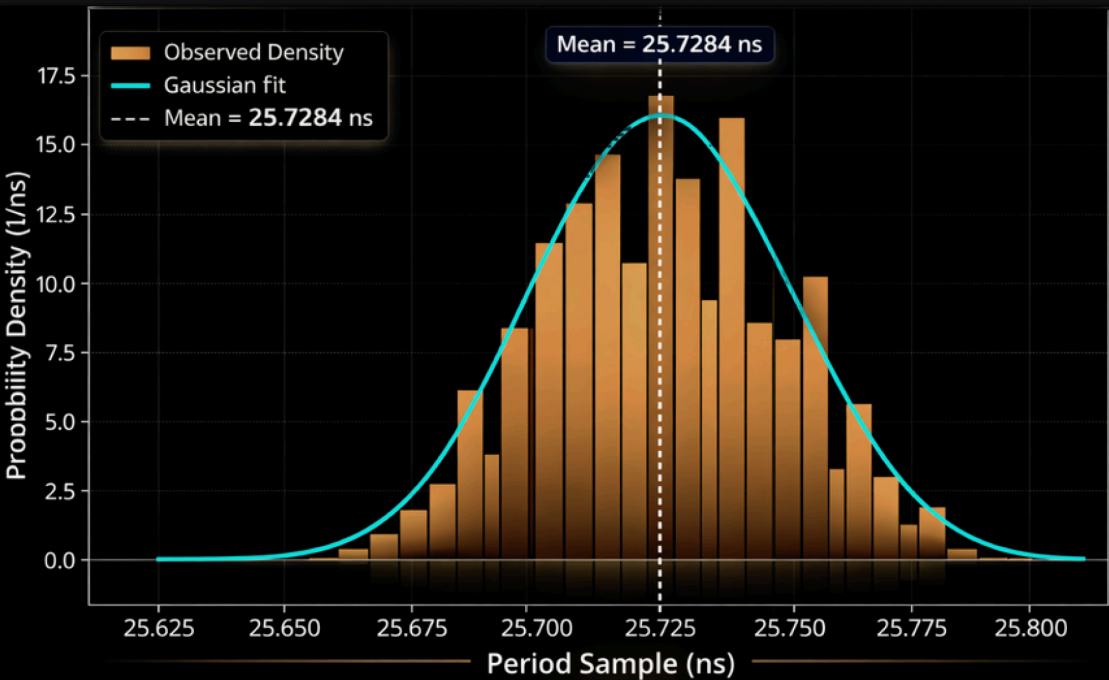
1PPS Outputs	4 × COAX (A1-A4)
10 MHz Outputs	4 × COAX (A1-A4)
1PPS Input	1 × COAX
10 MHz Input	1 × COAX
Calibration Port	1 × COAX

SYNCHRONISATION

Accuracy Class	Sub-nanosecond
Protocol	White Rabbit / PTP
WR Ports	4 × SFP

POWER & INTERFACE

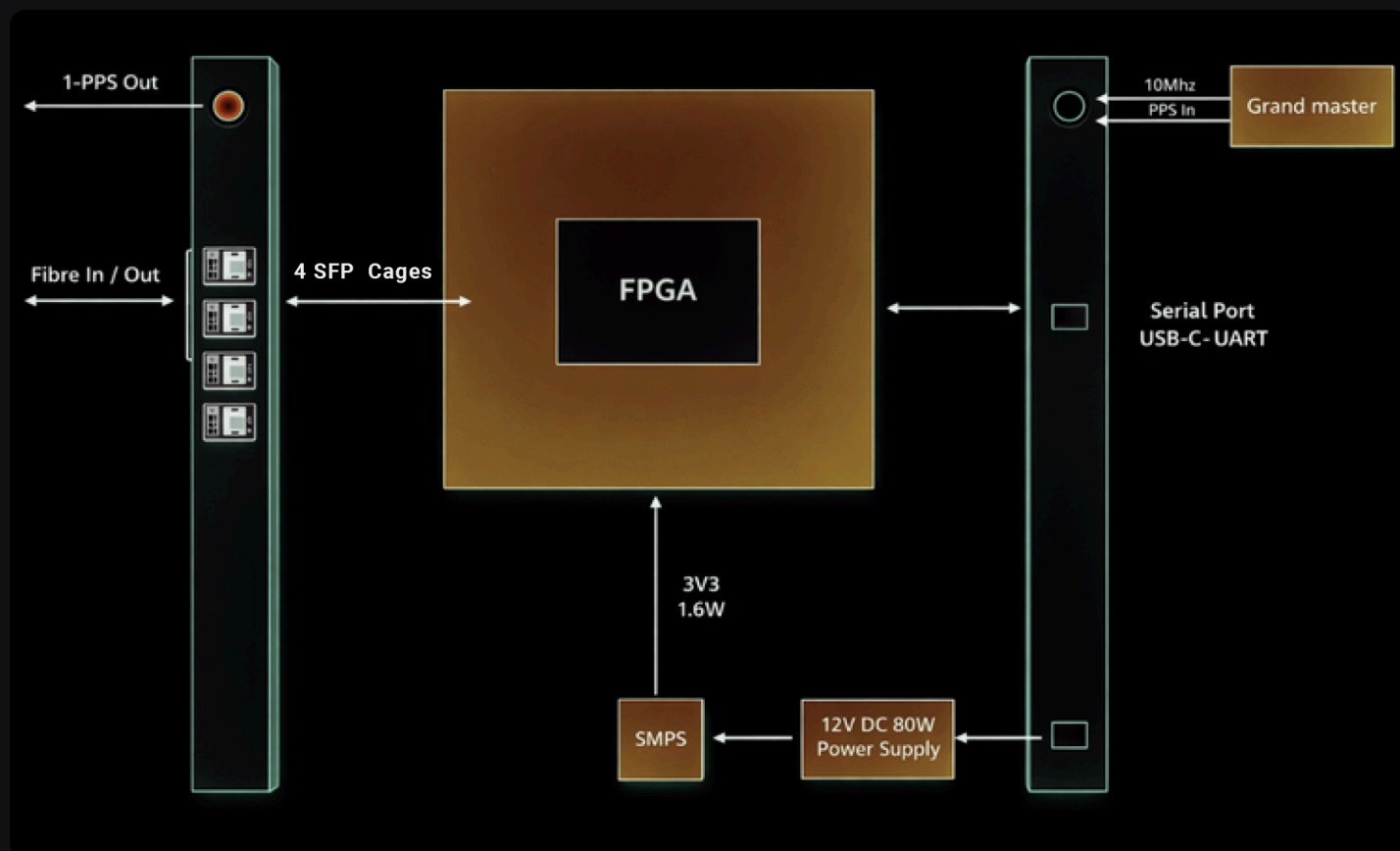
Power Input	12V DC (Barrel Jack)
Management	USB-C



CONNECTOR REFERENCE

CONNECTIONS

OPEN TIME NODE CONNECTIONS & 4 SFP CAGES



● CONNECTOR REFERENCE TABLE

REF	TYPE	FUNCTION
10M_IN	COAX	10 MHz input from grandmaster
CAL	COAX	Calibration input / Measurement port
PPS_IN	COAX	1PPS reference input from grandmaster
PPS_OUT (A1-A4)	COAX	1PPS outputs aligned to master when locked
10M_OUT (A1-A4)	COAX	10 MHz output, phase locked (PLL) to grandmaster
P12V	Barrel Jack	Primary power input 12V DC
USB	USB-C	Device management & configuration



HIGH-SPEED DIFFERENTIAL PAIRS

GPIO PINOUT

ROWS C & D — DATA & TIMING

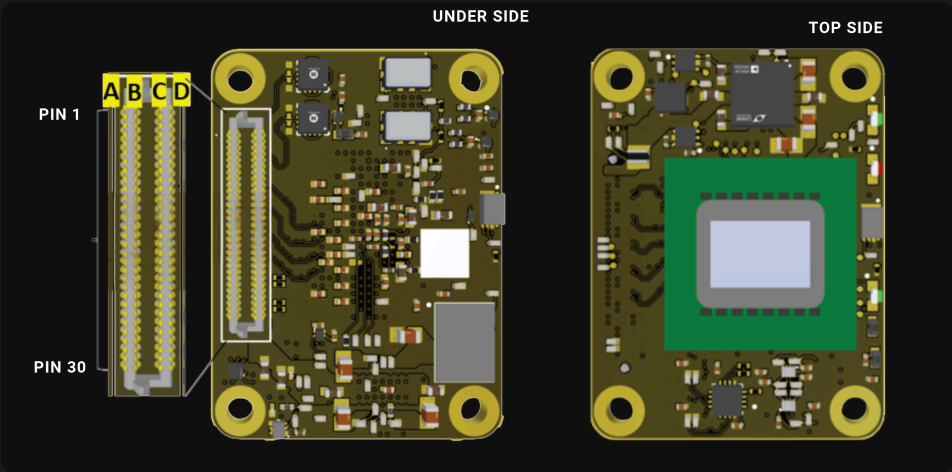
GPIO CONNECTOR (30-PIN × 4 ROWS: A, B, C, D)

Row A — Control & I2C

CLKGEN_SCL/SDA	I2C clock gen
SFP0-3 SDA/SCL	I2C per SFP
JTAG (TCK/TMS/TDO/TDI)	Debug interface
WR_UART TX/RX	WR UART
GNSS TX/RX	GNSS serial

Row B — Status & Signals

WR_PPS_3V3_IN	3V3 1PPS input
WR_ABSCAL_3V3_OUT	Abs. calibration
SFP0-3 TXDIS	TX disable
SFP0-3 MODABS	Module detect
SFP0-3 LOS	Loss of signal



ROW C — TIMING & RX

WR_PPS_OUT_N/P	PPS diff pair
WR_PPS_3V3_OUT	3V3 PPS output
WR_10M_3V3_OUT	3V3 10 MHz out
SFP0 RX_N/P	SFP0 receive
SFP1 RX_N/P	SFP1 receive
SFP2 RX_N/P	SFP2 receive
SFP3 RX_N/P	SFP3 receive
PCIE_FPGA_RX_N/P	PCIE RX pair

ROW D — TIMING & TX

WR_10M_3V3_IN	3V3 10 MHz in
WR_10M_OUT_N/P	10 MHz diff pair
SFP0 TX_N/P	SFP0 transmit
SFP1 TX_N/P	SFP1 transmit
SFP2 TX_N/P	SFP2 transmit
SFP3 TX_N/P	SFP3 transmit
PCIE_FPGA_TX_N/P	PCIE TX pair
PCIE_FPGA_REF_N/P	PCIE ref clock

POWER PINS

A30, B30, C30	P12V_IN (12V)
A14	P3V3_FPGA_EN
D30	GND



